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Design of low power pipelined ADC

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Abstract: A design of 8 bits, 2.5V pipeline ADC is introduced in this paper. The comparator is the main improvement aiming at realizing low power dissipation. The latched comparator is adopted to achieve the specification. The design is implemented under 0.25um CMOS technology which achieves a power dissipation of 205.9mW.

Keywords: Comparator, Op-amp, SUB-ADC, MDAC, SNDR, ENOB

I. INTRODUCTION

Pipelined analog-to-digital(ADC)architecture has gained great popularity in data communication and video processing applications where high sampling rates and medium-to-high resolutions are necessary Due to the increasing demand for portability in these applications, reducing the power consumption of ADC has become one of the key design criteria. While the pipelined ADC architecture is well suited for high sampling rates, reducing the power consumption .The proposed architecture consists by means of 4 separate 2 bit ADC sub-blocks, 1 MDAC block and 1 SHA block

II. PIPELINED ADC

Pipeline ADCs are also high speed ADCs and can be capable of resolving medium to high resolutions. [1] These ADCs work by converting a signal from analog to digital in stages. Each stage converts a portion of the output resolution. The first stage converts the most significant bits (MSB) and the subsequent stages convert less significant bits until the least significant bits (LSB) are converted. The overall general architecture of a pipeline ADC is shown in Figure 1. Each stage has a similar structure, shown exploded in Figure1. Each block contains a sample and hold block to sample the analog signal. This feeds into a small flash converter that resolves n-bits. This n-bit output is fed back through a DAC and the binary value is subtracted from the original input signal to generate a residue voltage.

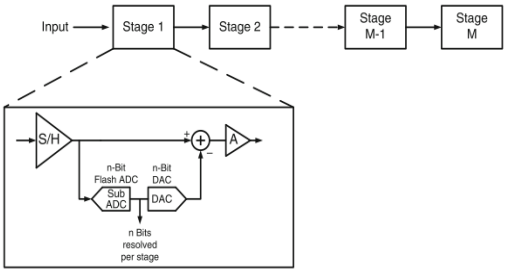

Figure1: Pipelined ADC

III. PROPOSED DESIGNS

A) *Proposed Comparator*

For the pipelined ADCs latched comparator is used. When ϕ_{latch} goes high 1, the gain transistors gets turn on, it amplifies the differential signal at the inputs V_{in} which is further amplified by the positive feedback action of the latch as the comparator goes into latch mode. The latch output is then applied to inverters sized in such a way as to lower the threshold point to prevent errors of comparator [4].Outputs of ADC remains 0 until the comparator has sufficient overdrive voltage to cause one output to toggle high. For resolution lower than 3 bits, dynamic comparators can be used for the inter-stage ADCs since they do not consume dc power. ADC will need to be preceded by continuous time preamplifiers to reduce the switch charge injection on the input signal and reference voltages V_{REF}. Figure 2 shows the CMOS implementation of comparator.

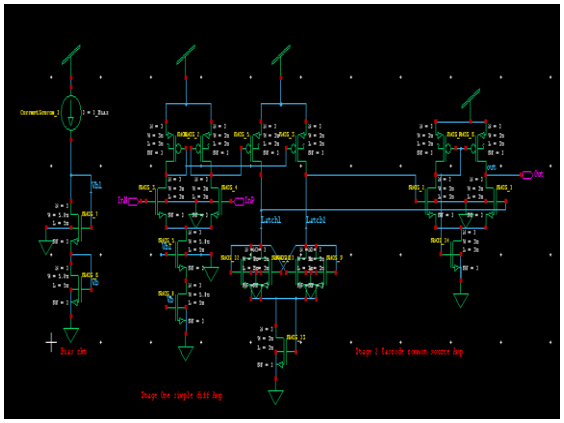

Figure 2: Schematic of comparator

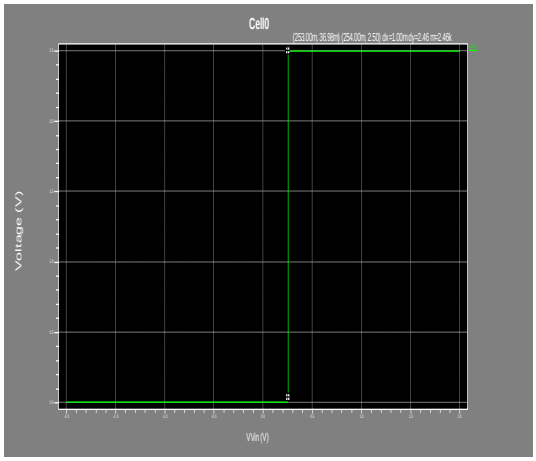

Figure 3: Output of comparator

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Table I:
Various parameters and their values

S. No.	Parameter	Value
1	DC gain	2372
2	Offset Voltage	1.38mW
3	Power Dissipation	4.023 µW

The design implementation of comparator consists of a latch stage preceded by coupling capacitors that are pre-charge to the input signal and reference voltages during the reset phase 4.023 microwatt dc power is dissipating in this comparator.

B) Proposed MDAC

MDAC (multiplying digital to anlog converters) commonly used in pipelined ADC's . Digital calibration technique is implemented in MDAC.Figure 4 shows the dsign of Multiplying digital to analog converter.

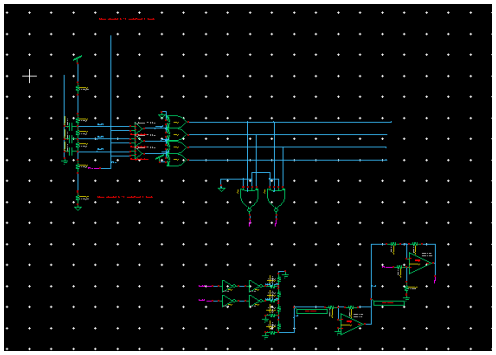

Figure 4: Schematic of MDAC

C) Proposed Op-amp

The op-amp is used in the MDAC to implement the stage gain. It's configured in a closed-loop circuit where the closed-loop gain is equal to the stage gain. The three op-amp design parameters that are discussed next are gain, bandwidth, and output swing.

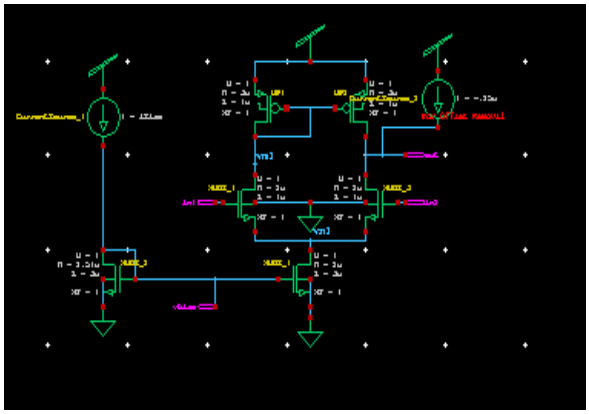

Figure 5: Cascode Op-amp

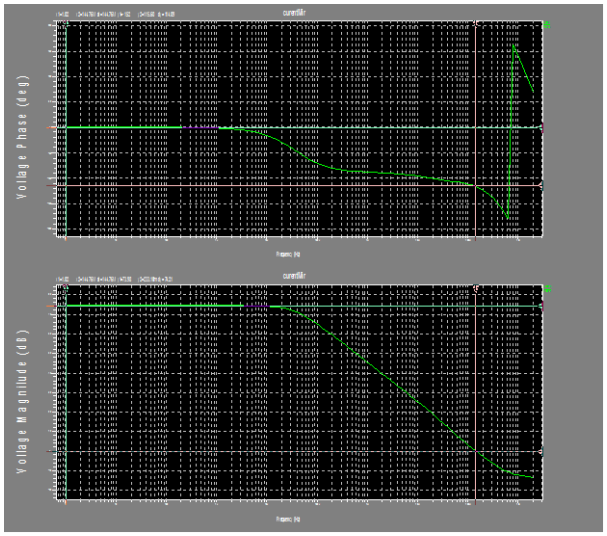

Figure 6: Op-amp characteristics

Table II:
Various parameters and their values

S.No.	Parameter	Value
1	AC Gain	81.52 dB
2	Phase Margin	69º
3	Unity Gain Bandwidth product	162.61 MHz
4	Power dissipation	8.507 mW

IV CONCLUSION

This work presents a novel front end technique that significantly reduces the power consumption in the front end S/H. The goal of this dissertation is to design a low power consumption ADC .The goal is accomplished by designing a 2.5 V, 2 bit/stage 8-bit ADC by using Latched Comparator in MDAC. The ADC is designed in 0.25 µm CMOS process at 2.5 V supply. At an input frequency of 1 MHz and a sampling rate of 5 MS/s, it consumes a power of 205.9 mW with 39.41 dB SNDR, 6.25 ENOB, 2.3/-2.1 LSB INL and +0.85/-0.21 LSB DNL. Performance for proposed design has been summarized in tabular form shown in below table.

Table III: Performance summary

Technology	0.25 µm CMOS process
Resolution	8 bit
Supply Voltage	2.5 V
Conversion rate	5 MS/s
SNDR	39.41 dB
ENOB	6.25
INL/DNL	+2.3/-2.1 LSB/ +0.85/-0.21 LSB
Power	205.9 mW

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